Semiconductor loss estimation in an innovative global power converter designer

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Abstract

This paper proposes an approach to quickly evaluate semiconductor losses. This approach combines a fast solver with ideal switch models and detailed loss data stored in multidimensional lookup-tables. This alternative offers a good compromise between accuracy and speed. It is implemented in PowerForge®, an innovative software to benchmark different power semiconductor devices or topologies. Results comparing PLECS, PSIM and PowerForge to evaluate the accuracy is proposed.

1 Introduction

Designing power converter is mostly a trade-off between efficiency and power density. While power density is mainly driven by the passive elements and heatsink volume, the efficiency is mainly impacted by the semiconductor losses (conduction and switching). Estimating accurately the losses of these devices is crucial for the converter efficiency as well as for the volume of the heatsinks. Usually, this loss estimation is performed with simple equations or with detailed simulations. This paper describes an approach that combines ideal switch models with detailed loss data to provide an efficient and accurate alternative to detailed device simulations at a minimum cost. This approach is used in PowerForge® [1], which is an innovative software to benchmark different topologies (including multilevel topologies such as NPC, T-type, flying capacitor) and different power semiconductor devices.

This paper purpose is to detail how the losses are estimated and how accurate they are compared to time-based circuit simulation tools.

In a first section, the general principle of the approach is described which relies on several distinct mechanisms: a frequency domain solver to compute waveforms, a storage in lookup tables of the loss data for a given component and an iterative loop to compute the junction temperature and exact losses. In a second section, the generation of the loss data are detailed. In a third section, the results are compared to time-based circuit simulation tools PLECS® [2] and PSIM® [3].

2 General principle

The approach to compute semiconductor losses is based on two key steps to provide a fast evaluation of these losses as shown in Fig. 1:

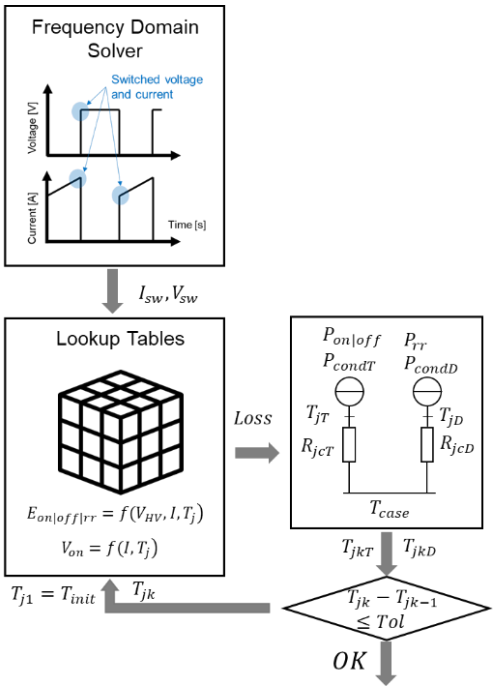

Fig. 1: General principle

- Steady-state waveforms of the whole circuit are directly determined thanks to a frequency domain solver adapted to the switching cell. From these waveforms are extracted the switched currents and voltages for each switch event.
- The values of current and voltage are used to read the resulting dissipated energy and power losses from multidimensional lookup tables for both conduction loss and switching loss.

The junction temperature considered is an average temperature over the modulation period. The losses and the junction temperature are determined with an iterative computation as the losses depend on the temperature and the temperature depends on the losses. This iterative loop ends when the difference of the junction temperature between two steps is below 0.5°C.

2.1 Steady-state Waveform Determination with a Frequency Solver

This method has been presented in [4]. The solver is adapted to commutation cells and based on the modified nodal analysis (MNA) [5]. It provides a very fast generic method to get steady-state waveforms of the power converters based on commutation cells with hard switching. The commutation cell is modelled by a current source I_{HV} at high voltage side and a voltage source V_{LV} at low voltage side as shown in Fig. 2 with the model of a simple dc-dc chopper.

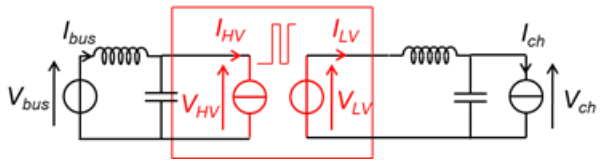

Fig. 2: Commutation cell model of a simple dc-dc chopper

The values of current source I_{HV} and voltage source V_{LV} are analytically computed from:

$$V_{LV}(t) = D(t) \cdot V_{HV}(t)$$
$$I_{HV}(t) = D(t) \cdot I_{LV}(t) \quad (1)$$

Where $D(t)$ is the duty cycle of the commutation cell.

The solving process can be summarized with the three steps shown in Fig. 3:

- The frequency spectrums of current I_{HV} and voltage V_{LV} are first obtained with the Fast Fourier Transform (FFT) algorithm.
- The MNA resolution is applied on all frequencies of the spectrum and the different voltages or currents of the circuits $(I_{LV}, V_{HV}, V_{ch}, I_{bus} \ldots)$ are determined.
- The Inverse Fast Fourier Transform (IFFT) algorithm is used to reconstruct the time-domain quantities at both sides of the commutation cell.

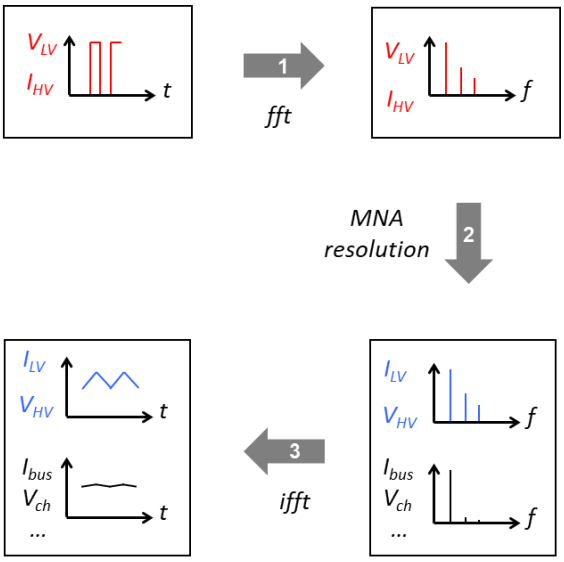

Fig. 3: Frequency resolution adapted to the commutation cell

From these waveforms are extracted the switched values of current and voltage as shown in Fig. 4.

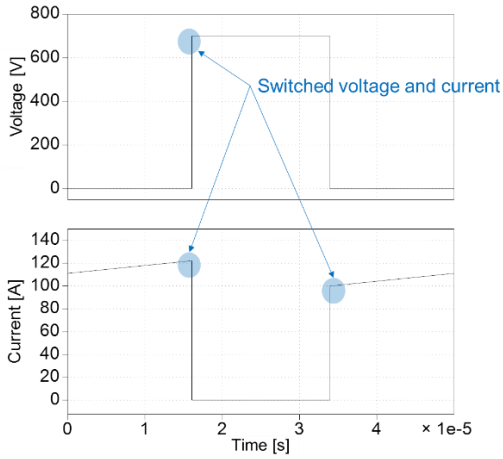

Fig. 4: Switched power and current

2.2 Loss Data Storage with Multidimensional Lookup Tables

Switching energy and voltage drop data are stored as multidimensional lookup tables for each power semiconductor device, as following:

$$E_{on|off|rr} = f(V_{HV}, I, T_j) \quad (2)$$

$$V_{on} = f(I, T_j) \quad (3)$$

A linear interpolation can be performed between the points stored in the lookup tables, resulting in a continuous surface presented in Fig. 5 for Eq° (2) and in continuous curves presented in Fig. 6 for Eq° (3). The lookup tables consider the dependence on the temperature, which is computed as an average temperature over a modulation period with the interaction of the cooling device. Loss data stored in these lookup tables are extracted from manufacturer datasheets or estimated with a SPICE model as presented in the following section.

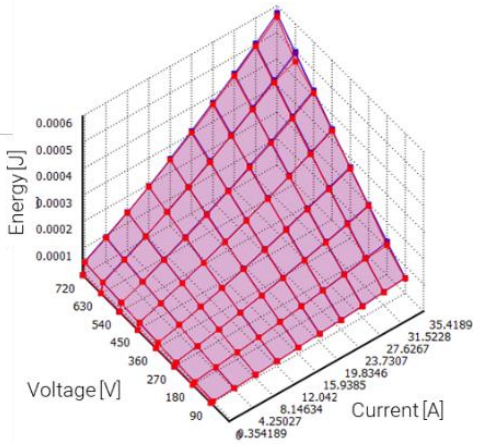

Fig. 5: Switching energies for different currents, voltages and temperatures

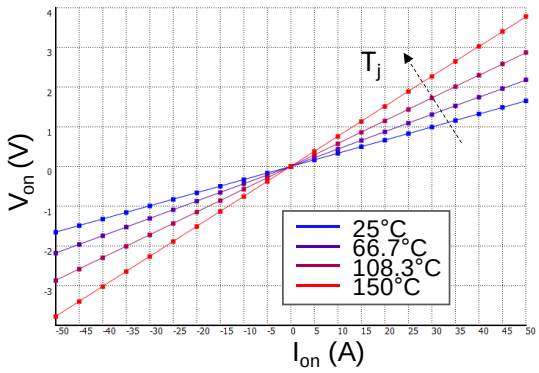

Fig. 6: Voltage drop for different current and temperatures (MOSFET)

3 Generation of Loss Data

3.1 Switching Loss Data

Switching energies, introduced in Eq° (2), are obtained by digitalizing the manufacturer datasheets, $E_{on|off|rr} = f(I)$ curves at different T_j are stored in the lookup tables. The switching energy is linearly interpolated or extrapolated especially for V_{HV}. If the manufacturers do not provide loss measurement results (i.e. low voltage Si-MOSFET), the authors developed a double-pulse SPICE simulation to estimate $E_{on|off|rr} = f(I, T_J, V_{DS})$. This last process will be detailed in next section.

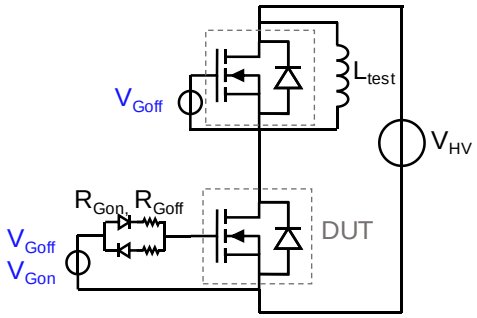

Fig. 7: Double pulse schematic

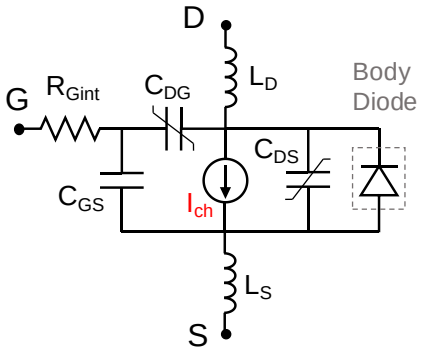

Fig. 8: MOSFET model

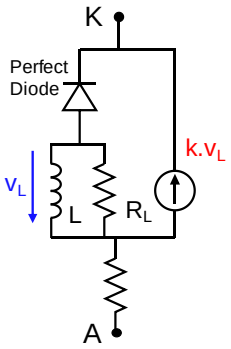

Fig. 9: Diode model

3.2 Switching Loss Data Generation for Si-MOSFETS

In this case, the switching energies are obtained by a double-pulse measurement SPICE simulation. The classical double pulse simulation schematic is presented in Fig. 7. The turn-on and turn-off voltages are the nominal ones from the manufacturer datasheet. The pulse times are swept in order to obtain the switching energies for a large panel of drain currents as well as gate

resistors and bus voltages (V_{HV}). The model of the device under test (DUT), including the body diode, is based on [6]. The schematic of the MOSFET and the body diode are presented in Fig. 8 and Fig. 9.

The MOSFET drain current is described with the following equations:

$$I_{ch} = sign(V_{DS}) \cdot \min\left(I_{pot}, \left|\frac{V_{DS}}{R_{DSon}}\right|\right) \quad (4)$$

With:

$$\begin{aligned} &if\ (V_{GS} - V_{th}) > 0, \\ &I_{pot} = K_p \cdot (V_{GS} - V_{th})^2 \\ &else\ I_{pot} = 0 \end{aligned} \quad (5)$$

and K_p the transconductance parameter, R_{DSon} the channel resistance, V_{th} the threshold voltage.

All the parameters are extracted from the manufacturer datasheet in particular $C_{DG}(V_{DS})$ and $C_{DS}(V_{DS})$.

The body diode recovery current is modeled by identifying three parameter values L, R_L and k based on the MOSFET electrical characteristics (I_{RRM}, Q_R) as described in [6].

The temperature dependence is possible if the parameters are given for different temperatures.

3.3 Conduction Loss Data

Voltage drops, introduced in Eq° (3), for computing conduction loss are obtained by digitalizing the manufacturer datasheets, typically $R_{DS(on)} = f(T_j)$ curves for MOSFET and $I(V)$ curves at different T_j for IGBT and diodes. These curves are always taken at nominal gate drive voltage.

3.4 Reverse conduction of MOSFETS with or without external diode

When conducting reverse current, synchronous rectification is used if the transistor's technology makes it possible (e.g. MOSFET). The transistor gate is assumed to be driven high, so that the channel can contribute to reverse current conduction. In this case, the reverse current may be split between controlled and spontaneous reverse conduction mechanisms (e.g. diode and channel) in a ratio that depends on total reverse current and on each junction temperature as illustrated in Fig. 10. The proposed approach handles this and pre-computes the conduction ratio between the two conduction mechanisms as shown in Fig. 11.

Fig. 12 shows the different device contributions in reverse conduction and the resulting voltage drop depending on the total current. This result shows the benefit of the diode conduction at high current level for Si-MOSFET.

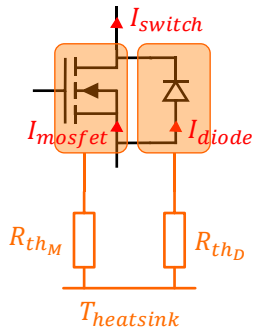

Fig. 10: Thermal model and current sharing between the couple MOSFET and diode

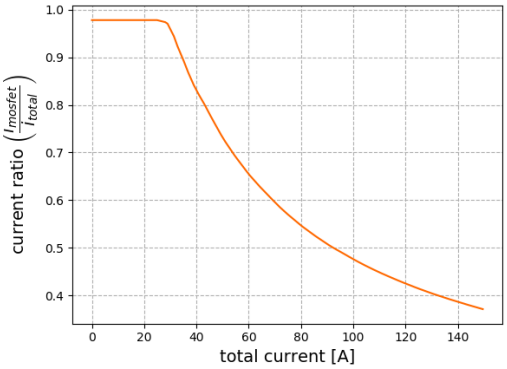

Fig. 11: Current ratio pre-computed as a function of the current

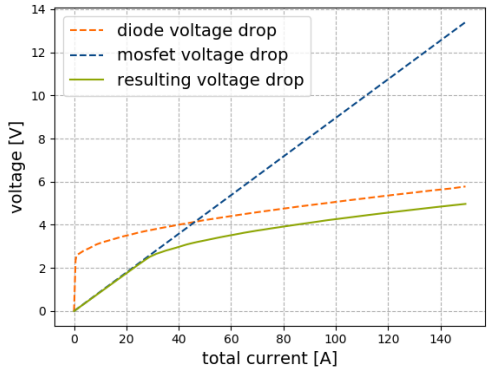

Fig. 12: Voltage drop contributions in reverse conduction of MOSFET and diode

4 Results and Comparison

The proposed approach is implemented in a computer-aided engineering platform dedicated to benchmark different power semiconductor devices or topologies for power converter design: Powerforge®[1].

The losses are compared between PowerForge, PLECS [2] and PSIM [3] software for three cases:

- a DC-DC conversion stage composed of two 3-level flying capacitor switching cells in parallel ($n_{cell(FC)}$=2 and $n_{cell(par)}$=2) ,
- a 2-level 3-phase inverter,
- a motor drive application where two topologies are compared: a 3-level T-type and a 3-level flying capacitor.

The comparison of the results shows the sum of the losses in the diode and the transistor for switching and conduction losses, junction temperatures of each device and the relative errors. The semiconductors losses curves have been extracted from the manufacturers datasheet for different temperatures as explained above.

4.1 Case 1: DC-DC conversion stage

This conversion stage is composed of two flying capacitor cells connected in parallel and interleaved as shown in **Erreur ! Source du renvoi introuvable.**.

The characteristics of this conversion stage are presented in Table 1.

Table 1: Parameters of the DC-DC conversion stage

Switch reference	IKB20N60H3
$R_{th(c-s)}$ per switch	1.14 K / W
$R_{th(s-a)}$	0.2 K / W
$T_{ambient}$	25 °C
V_{HV}	450 V
V_{LV}	300 V
i_{LV}	40 A
$n_{cell(FC)}$	2
$n_{cell(par)}$	2
f_{sw}	10 kHz
C_{fly}	297 µF
L_{LV}	100 µH
$R_{winding\ L}$	1 mΩ
C_{LV}	1 mF

A first comparison of the iterative thermal computation has been performed using waveforms generated by PLECS and have been re-injected in PowerForge to compute the losses and the junction temperatures. This comparison showed a relative error below 10^{-5}, due to the convergence of the thermal computation in PowerForge. Indeed, this thermal computation includes an iterative loop (Fig. 1) which ends with a small tolerance on the junction temperature between two computation steps.

A full comparison has then been performed between PowerForge, PLECS and PSIM and results are shown in Table 2.

Table 2: Comparison results for the DC-DC conversion stage between PowerForge, PLECS and PSIM

	PF	PLECS		PSIM	
	Value	**Value**	**Δ(%)**	**Value**	**Δ(%)**
$P_{sw(High)}$ [W]	4.62	4.6	0.4	4.36	5.6
$P_{cond(High)}$ [W]	31.30	31.2	0.3	31.25	0.2
$P_{cond(Low)}$ [W]	15.10	15.10	0	15.10	0
$P_{sw(Low)}$ [W]	0	0	0	0	0
$T_{j(T-High)}$ [°C]	138.4	138.9	0.4	137.6	0.6
$T_{j(D-High)}$ [°C]	106.9	107.4	0.5	106.3	0.3
$T_{j(T-Low)}$ [°C]	83.1	83.6	0.6	82.8	0.5
$T_{j(D-Low)}$ [°C]	111.7	112.3	0.5	111.4	0.6

Most of difference are below 1% except for the switching losses computed with PSIM. These small differences can be explained with the differences between the currents and voltages switched values which are computed with different solvers.

4.2 Case 2: 2-level 3-phase inverter

The second comparison is based on a 2 level 3-Phase inverter as shown in Fig. 13. The characteristics of this second comparison case are shown in Table 1.

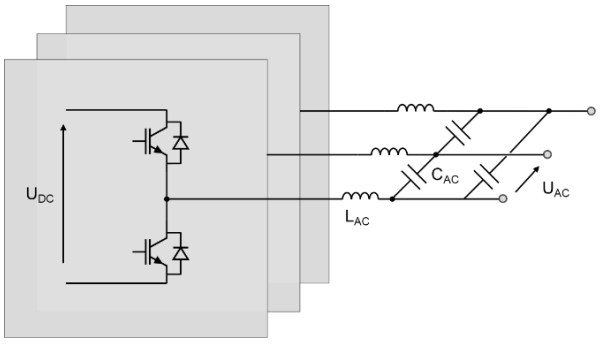

Fig. 13 Circuit of a 2-Level 3-phase inverter

The comparison results of the second case are shown in Table 4. Switching and conduction losses are the sum of transistor and conduction losses.

In this case of a 3-phase inverter, where the HF current ripple is only 20% peak-to-peak, the influence of the solver on the waveforms and on the values of the switched currents is less important. Thus, PSIM simulation shows closer results than in previous case. Moreover, PSIM performs an averaged thermal computation on the modulation period in the same way as PowerForge and shows closer results than PLECS, which

dynamically computes the junction temperatures with the instantaneous loss computation.

Table 3: Parameters of the 2-level 3-phase inverter

Switch reference	FGH12040WD
$R_{th(c-s)}$ per switch	1.14 K / W
$R_{th(s-a)}$	0.2 K / W
$T_{ambient}$	25 °C
U_{DC}	750 V
$U_{AC\ RMS}$	400 V
P_{AC}	20 kW
f_0	50 Hz
f_{sw}	10 kHz
L_{AC}	1.27 mH
$R_{winding\ L}$	0.24 Ω
C_{AC}	14.9 mF

Table 4: Comparison results for the 2-Level 3-phase inverter between PowerForge, PLECS and PSIM

	PF	PLECS		PSIM	
	Value	Value	Δ(%)	Value	Δ(%)
P_{sw} [W]	25.81	25.76	0.2	25.83	0.07
P_{cond} [W]	29.60	29.59	0.04	29.62	0.06
$T_{j(T)}$ [°C]	150.1	149.8	0.2	150.2	0.06
$T_{j(D)}$ [°C]	139.2	138.8	0.3	139.2	0

4.3 Case 3: Motor drive application

At last, the losses of a T-type inverter, shown in Fig. 14, for a motor drive application are compared:

- Power: 200 kW,
- Phase-to-phase voltage: 690 V AC.

The characteristics of the T-type inverter are shown in Table 5.

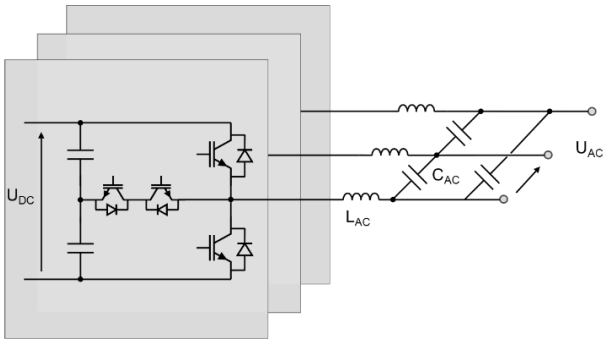

Fig. 14 Circuit of a T-Type 3-phase inverter

In this case, again, PLECS simulation shows différence that are a little bit higher than PSIM simulation, which is due to the different process of the thermal computation.

Table 5: Parameters of the 3-level T-type inverter

Module reference	SEMiX305TMLI17E4C
$R_{th(c-s)}$ per switch	0.018 K / W
$R_{th(s-a)}$	0.072 K / W
$T_{ambient}$	25 °C
U_{DC}	1070 V
$U_{AC\ RMS}$	690 V
P_{AC}	200 kW
f_0	50 Hz
f_{sw}	2.5 kHz
L_{AC}	211e-6 µH
$R_{winding\ L}$	0.07 Ω
C_{AC}	26.9 mF

Table 6 : semiconductor losses for two topologies estimated with three software

	PF	PLEC		PSIM	
	Value	Value	Δ(%)	Value	Δ(%)
$P_{sw(inner)}$ [W]	10.1	9.4	7	10.2	1
$P_{sw(outer)}$ [W]	55.1	55.1	0	55.4	0.5
$P_{cond(inner)}$ [W]	36.1	36.1	0	36.1	0
$P_{cond(outer)}$ [W]	129.5	129.7	0.2	129.3	0.2
$T_{j(T\ inner)}$	129.8	128.4	1	129.9	0.08
$T_{j(T\ outer)}$	149.9	148.5	1	150.0	0.07
$T_{j(D\ inner)}$	133.7	132.2	1	133.9	0.1
$T_{j(D\ outer)}$	135.2	133.8	1	135.3	0.07

5 Conclusion

This paper presents a fast and accurate method to estimate semiconductor losses in various power converter topologies. The fast frequential solver is used to determine waveforms, i.e. the switched voltages and currents and the currents through the devices. Therefore, these quantities are used to read lookup tables to evaluate switching and conduction losses and each chip temperature. The lookup table data are extracted from the manufacturer datasheets or estimated with a double-pulse measurement of a SPICE simulation (typically for low-voltage Si-MOSFETS). Finally, the described approach is compared with two well-known simulation tools, PSIM® and PLECS® showing a good accuracy with a maximum difference - for the considered examples - below 1% for PSIM and maximum 7% for PLECS. The differences can be explained:

- from the different solvers which are used (between PLECS, PSIM and PowerForge)

which can give different values of the switched current and voltages,
- from the different processes of the thermal computation. On one side, PSIM and PowerForge perform a thermal computation of averaged junction temperature over a modulation period. On the other side, PLECS dynamically computes the junction temperatures with the instantaneous loss computation.

Thus, PSIM and PowerForge gives closer results than PLECS and PowerForge.

This approach is based on the frequential solver previously described that is much faster than time solvers. Losses evaluation is, therefore, quicker for a huge number of different power converter solutions. This technological advance is paving the way for power converter design automation.

6 Références

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